WHAT IS CLAIMED IS:

1. A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region;

a gate electrode formed on the gate insulation film;

a source electrode connected electrically to the source region;

an insulation film on the drift region and adjacent to the gate electrode; and

a field plate on the insulation film, the field plate being connected to the source electrode.

2. The MIS-type semiconductor device according to claim 1, further including an interlayer insulation film insulating the gate electrode and the source electrode from each other, wherein the insulation film is thinner than the interlayer insulation film.

3. The MIS-type semiconductor device according to claim 1, wherein the insulation film is as thin as or thicker than the gate insulation film and as thick as or thinner than Vb/Ec, where Vb is the breakdown voltage of the MIS-type semiconductor device and Ec is the critical dielectric breakdown strength of silicon.

4. The MIS-type semiconductor device according to claim 1, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

5. The MIS-type semiconductor device according to claim 2, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate

electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

6. The MIS-type semiconductor device according to claim 3, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

7. The MIS-type semiconductor device according to claim 4, wherein the second drift region is larger in volume than the first drift region.

8. The MIS-type semiconductor device according to claim 5, wherein the second drift region is larger in volume than the first drift region.

9. The MIS-type semiconductor device according to claim 6, wherein the second drift region is larger in volume than the first drift region.

10. The MIS-type semiconductor device according to claim 4, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

11. The MIS-type semiconductor device according to claim 5, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

12. The MIS-type semiconductor device according to claim 6, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

13. The MIS-type semiconductor device according to claim 7, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

14. The MIS-type semiconductor device according to claim 8, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

15. The MIS-type semiconductor device according to claim 9, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

16. The MIS-type semiconductor device according to claim 4, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

17. The MIS-type semiconductor device according to claim 5, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

18. The MIS-type semiconductor device according to claim 6, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

19. The MIS-type semiconductor device according to claim 7, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

20. The MIS-type semiconductor device according to claim 8, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

21. The MIS-type semiconductor device according to claim 9, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

22. The MIS-type semiconductor device according to claim 10, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

23. The MIS-type semiconductor device according to claim 11, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

24. The MIS-type semiconductor device according to claim 12, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

25. The MIS-type semiconductor device according to claim 13, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

26. The MIS-type semiconductor device according to claim 14, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

27. The MIS-type semiconductor device according to claim 15, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

28. The MIS-type semiconductor device according to claim 4, further including a drain region spaced from the first drift region.

29. The MIS-type semiconductor device according to claim 5, further including a drain region spaced from the first drift region.

30. The MIS-type semiconductor device according to claim 6, further including a drain region spaced from the first drift region.

31. The MIS-type semiconductor device according to claim 7, further including a drain region spaced from the first drift region.

32. The MIS-type semiconductor device according to claim 8, further including a drain region spaced from the first drift region.

33. The MIS-type semiconductor device according to claim 9, further including a drain region spaced from the first drift region.

34. The MIS-type semiconductor device according to claim 10, further including a drain region spaced from the first drift region.

35. The MIS-type semiconductor device according to claim 11, further including a drain region spaced from the first drift region.

36. The MIS-type semiconductor device according to claim 12, further including a drain region spaced from the first drift region.

37. The MIS-type semiconductor device according to claim 13, further including a drain region spaced from the first drift region.

38. The MIS-type semiconductor device according to claim 14, further including a drain region spaced from the first drift region.

39. The MIS-type semiconductor device according to claim 15, further including a drain region spaced from the first drift region.

40. The MIS-type semiconductor device according to claim 16, further including a drain region spaced from the first drift region.

41. The MIS-type semiconductor device according to claim 17, further including a drain region spaced from the first drift region.

42. The MIS-type semiconductor device according to claim 18, further including a drain region spaced from the first drift region.

43. The MIS-type semiconductor device according to claim 19, further including a drain region spaced from the first drift region.

44. The MIS-type semiconductor device according to claim 20, further including a drain region spaced from the first drift region.

45. The MIS-type semiconductor device according to claim 21, further including a drain region spaced from the first drift region.

46. The MIS-type semiconductor device according to claim 22, further including a drain region spaced from the first drift region.

47. The MIS-type semiconductor device according to claim 23, further including a drain region spaced from the first drift region.

48. The MIS-type semiconductor device according to claim 24, further including a drain region spaced from the first drift region.

49. The MIS-type semiconductor device according to claim 25, further including a drain region spaced from the first drift region.

50. The MIS-type semiconductor device according to claim 26, further including a drain region spaced from the first drift region.

51. The MIS-type semiconductor device according to claim 27, further including a drain region spaced from the first drift region.

52. A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region between the source region and the drift region; and

a gate electrode formed on the gate insulation film;

wherein the base region in contact with the gate insulation film has an impurity concentration peak positioned more closely to the drift region than to the source region.

53. The MIS-type semiconductor device according to claim 52, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

54. The MIS-type semiconductor device according to claim 53, wherein the second drift region is larger in volume than the first drift region.

55. The MIS-type semiconductor device according to claim 53, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

56. The MIS-type semiconductor device according to claim 54, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

57. The MIS-type semiconductor device according to claim 53, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

58. The MIS-type semiconductor device according to claim 54, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

59. The MIS-type semiconductor device according to claim 55, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

60. The MIS-type semiconductor device according to claim 56, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

61. The MIS-type semiconductor device according to claim 53, further including a drain region spaced from the first drift region.

62. The MIS-type semiconductor device according to claim 54, further including a drain region spaced from the first drift region.

63. The MIS-type semiconductor device according to claim 55, further including a drain region spaced from the first drift region.

64. The MIS-type semiconductor device according to claim 56, further including a drain region spaced from the first drift region.

65. The MIS-type semiconductor device according to claim 57, further including a drain region spaced from the first drift region.

66. The MIS-type semiconductor device according to claim 58, further including a drain region spaced from the first drift region.

67. The MIS-type semiconductor device according to claim 59, further including a drain region spaced from the first drift region.

68. The MIS-type semiconductor device according to claim 60, further including a drain region spaced from the first drift region.

69. A MIS-type semiconductor device comprising:

a source region of a first conductivity type;

a base region of a second conductivity type;

a drift region of the first conductivity type;

a gate insulation film on the base region between the source region and the drift region;

a gate electrode on the gate insulation film interposed therebetween; and

a heavily doped region of the second conductivity type in the base region below the gate electrode,

wherein the heavily doped region positioned between the source region and the drift region to enable a depletion layer expanding from the drift region into the base region reach the heavily doped region.

70. The MIS-type semiconductor device according to claim 69, wherein an edge of the heavily doped region being spaced apart 2.5 μm or narrower from the gate insulation film and for 5.6 μm or narrower from the drift region.

71. The MIS-type semiconductor device according to claim 69, wherein the edge of the heavily doped region is spaced apart for 1 μm or narrower from the gate insulation film.

72. The MIS-type semiconductor device according to claim 70, wherein the edge of the heavily doped region is spaced apart for 1 μm or narrower from the gate insulation film.

73. The MIS-type semiconductor device according to claim 69, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

74. The MIS-type semiconductor device according to claim 70, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

75. The MIS-type semiconductor device according to claim 71, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

76. The MIS-type semiconductor device according to claim 72, wherein the drift region comprises a first drift region and a second drift region, the first region being doped heavier than the second drift region, at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and an edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

77. The MIS-type semiconductor device according to claim 73, wherein the second drift region is larger in volume than the first drift region.

78. The MIS-type semiconductor device according to claim 74, wherein the second drift region is larger in volume than the first drift region.

79. The MIS-type semiconductor device according to claim 75, wherein the second drift region is larger in volume than the first drift region.

80. The MIS-type semiconductor device according to claim 76, wherein the second drift region is larger in volume than the first drift region

81. The MIS-type semiconductor device according to claim 73, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

82. The MIS-type semiconductor device according to claim 74, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

83. The MIS-type semiconductor device according to claim 75, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

84. The MIS-type semiconductor device according to claim 76, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

85. The MIS-type semiconductor device according to claim 77, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

86. The MIS-type semiconductor device according to claim 78, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

87. The MIS-type semiconductor device according to claim 79, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

88. The MIS-type semiconductor device according to claim 80, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

89. The MIS-type semiconductor device according to claim 73, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

90. The MIS-type semiconductor device according to claim 74, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

91. The MIS-type semiconductor device according to claim 75, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

92. The MIS-type semiconductor device according to claim 76, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

93. The MIS-type semiconductor device according to claim 77, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

94. The MIS-type semiconductor device according to claim 78, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

95. The MIS-type semiconductor device according to claim 79, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

96. The MIS-type semiconductor device according to claim 80, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

97. The MIS-type semiconductor device according to claim 81, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

98. The MIS-type semiconductor device according to claim 82, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

99. The MIS-type semiconductor device according to claim 83, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

100. The MIS-type semiconductor device according to claim 84, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

101. The MIS-type semiconductor device according to claim 85, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

102. The MIS-type semiconductor device according to claim 86, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

103. The MIS-type semiconductor device according to claim 87, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

104. The MIS-type semiconductor device according to claim 88, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

105. The MIS-type semiconductor device according to claim 73, further including a drain region spaced from the first drift region.

106. The MIS-type semiconductor device according to claim 74, further including a drain region spaced from the first drift region.

107. The MIS-type semiconductor device according to claim 75, further including a drain region spaced from the first drift region.

108. The MIS-type semiconductor device according to claim 76, further including a drain region spaced from the first drift region.

109. The MIS-type semiconductor device according to claim 77, further including a drain region spaced from the first drift region.

110. The MIS-type semiconductor device according to claim 78, further including a drain region spaced from the first drift region.

111. The MIS-type semiconductor device according to claim 79, further including a drain region spaced from the first drift region.

112. The MIS-type semiconductor device according to claim 80, further including a drain region spaced from the first drift region.

113. The MIS-type semiconductor device according to claim 81, further including a drain region spaced from the first drift region.

114. The MIS-type semiconductor device according to claim 82, further including a drain region spaced from the first drift region.

115. The MIS-type semiconductor device according to claim 83, further including a drain region spaced from the first drift region.

116. The MIS-type semiconductor device according to claim 84, further including a drain region spaced from the first drift region.

117. The MIS-type semiconductor device according to claim 85, further including a drain region spaced from the first drift region.

118. The MIS-type semiconductor device according to claim 86, further including a drain region spaced from the first drift region.

119. The MIS-type semiconductor device according to claim 87, further including a drain region spaced from the first drift region.

120. The MIS-type semiconductor device according to claim 88, further including a drain region spaced from the first drift region.

121. The MIS-type semiconductor device according to claim 89, further including a drain region spaced from the first drift region.

122. The MIS-type semiconductor device according to claim 90, further including a drain region spaced from the first drift region.

123. The MIS-type semiconductor device according to claim 91, further including a drain region spaced from the first drift region.

124. The MIS-type semiconductor device according to claim 92, further including a drain region spaced from the first drift region.

125. The MIS-type semiconductor device according to claim 93, further including a drain region spaced from the first drift region.

126. The MIS-type semiconductor device according to claim 94, further including a drain region spaced from the first drift region.

127. The MIS-type semiconductor device according to claim 95, further including a drain region spaced from the first drift region.

128. The MIS-type semiconductor device according to claim 96, further including a drain region spaced from the first drift region.

129. The MIS-type semiconductor device according to claim 97, further including a drain region spaced from the first drift region.

130. The MIS-type semiconductor device according to claim 98, further including a drain region spaced from the first drift region.

131. The MIS-type semiconductor device according to claim 99, further including a drain region spaced from the first drift region.

132. The MIS-type semiconductor device according to claim 100, further including a drain region spaced from the first drift region.

133. The MIS-type semiconductor device according to claim 101, further including a drain region spaced from the first drift region.

134. The MIS-type semiconductor device according to claim 102, further including a drain region spaced from the first drift region.

135. The MIS-type semiconductor device according to claim 103, further including a drain region spaced from the first drift region.

136. The MIS-type semiconductor device according to claim 104, further including a drain region spaced from the first drift region.

137. A MIS-type semiconductor device comprising:
a source region of a first conductivity type;
a base region of a second conductivity type;

a drift region of the first conductivity type comprised of a first drift region and a second drift region, the first drift region being doped heavier than the second drift region;

a gate insulation film on the base region; and

a gate electrode on the gate insulation film,

wherein at least a part of the surfaces of the first drift region and the gate electrode overlap each other, and

wherein the edge of the second drift region is positioned farther from the gate electrode than the first drift region so that the second drift region is not exposed to the surface of the base region beneath the gate electrode.

138. A MIS-type semiconductor device according to claim 137, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, and a drain region of the first conductivity type connected to the drift region, wherein the source region, the base region, and the drift region are on the side of the first major surface, and the drift region is spaced from the source region.

139. A MIS-type semiconductor device according to claim 137, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, and a drain region of the first conductivity type on the side of the second major surface, the drain region being connected to the drift region, wherein the source region, the base region, and the drift region are on the side of the first major surface, and the drift region is spaced apart from the source region.

140. A MIS-type semiconductor device according to claim 137, further including a semiconductor chip having a first major surface and a second major surface facing opposite to each other, a trench, and a drain region of the first conductivity type on the side of the second major surface, the drain region being connected to the drift region, wherein the base region and the source region are on the side of the first major surface, the trench is formed through the source region down to the base region, the gate electrode is in the trench or on the side wall of the trench with the gate insulation film interposed between the gate electrode and the trench, the

drift region is in contact with the bottom of the trench, the drift region is below the gate electrode so that the drift region overlaps with the gate electrode in the projection perpendicular to the second major surface.

141. The MIS-type semiconductor device according to claim 137, wherein the second drift region is larger in volume than the first drift region.

142. The MIS-type semiconductor device according to claim 138, wherein the second drift region is larger in volume than the first drift region.

143. The MIS-type semiconductor device according to claim 139, wherein the second drift region is larger in volume than the first drift region.

144. The MIS-type semiconductor device according to claim 140, wherein the second drift region is larger in volume than the first drift region.

145. The MIS-type semiconductor device according to claim 137, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

146. The MIS-type semiconductor device according to claim 138, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

147. The MIS-type semiconductor device according to claim 139, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

148. The MIS-type semiconductor device according to claim 140, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

149. The MIS-type semiconductor device according to claim 141, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

150. The MIS-type semiconductor device according to claim 142, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

151. The MIS-type semiconductor device according to claim 143, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

152. The MIS-type semiconductor device according to claim 144, wherein the diffusion depth of the second drift region is longer than the diffusion depth of the first drift region.

153. The MIS-type semiconductor device according to claim 137, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

154. The MIS-type semiconductor device according to claim 138, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

155. The MIS-type semiconductor device according to claim 139, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

156. The MIS-type semiconductor device according to claim 140, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

157. The MIS-type semiconductor device according to claim 141, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

158. The MIS-type semiconductor device according to claim 142, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

159. The MIS-type semiconductor device according to claim 143, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

160. The MIS-type semiconductor device according to claim 144, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

161. The MIS-type semiconductor device according to claim 145, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

162. The MIS-type semiconductor device according to claim 146, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

163. The MIS-type semiconductor device according to claim 147, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

164. The MIS-type semiconductor device according to claim 148, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

165. The MIS-type semiconductor device according to claim 149, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

166. The MIS-type semiconductor device according to claim 150, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

167. The MIS-type semiconductor device according to claim 151, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

168. The MIS-type semiconductor device according to claim 152, wherein the net impurity amount per a unit length in the second drift region is larger than the net impurity amount per a unit length in the first drift region.

169. The MIS-type semiconductor device according to claim 137, further including a drain region spaced from the first drift region.

170. The MIS-type semiconductor device according to claim 138, further including a drain region spaced from the first drift region.

171. The MIS-type semiconductor device according to claim 139, further including a drain region spaced from the first drift region.

172. The MIS-type semiconductor device according to claim 140, further including a drain region spaced from the first drift region.

173. The MIS-type semiconductor device according to claim 141, further including a drain region spaced from the first drift region.

174. The MIS-type semiconductor device according to claim 142, further including a drain region spaced from the first drift region.

175. The MIS-type semiconductor device according to claim 143, further including a drain region spaced from the first drift region.

176. The MIS-type semiconductor device according to claim 144, further including a drain region spaced from the first drift region.

177. The MIS-type semiconductor device according to claim 145, further including a drain region spaced from the first drift region.

178. The MIS-type semiconductor device according to claim 146, further including a drain region spaced from the first drift region.

179. The MIS-type semiconductor device according to claim 147, further including a drain region spaced from the first drift region.

180. The MIS-type semiconductor device according to claim 148, further including a drain region spaced from the first drift region.

181. The MIS-type semiconductor device according to claim 149, further including a drain region spaced from the first drift region.

182. The MIS-type semiconductor device according to claim 150, further including a drain region spaced from the first drift region.

183. The MIS-type semiconductor device according to claim 151, further including a drain region spaced from the first drift region.

184. The MIS-type semiconductor device according to claim 152, further including a drain region spaced from the first drift region.

185. The MIS-type semiconductor device according to claim 153, further including a drain region spaced from the first drift region.

186. The MIS-type semiconductor device according to claim 154, further including a drain region spaced from the first drift region.

187. The MIS-type semiconductor device according to claim 155, further including a drain region spaced from the first drift region.

188. The MIS-type semiconductor device according to claim 156, further including a drain region spaced from the first drift region.

189. The MIS-type semiconductor device according to claim 157, further including a drain region spaced from the first drift region.

190. The MIS-type semiconductor device according to claim 158, further including a drain region spaced from the first drift region.

191. The MIS-type semiconductor device according to claim 159, further including a drain region spaced from the first drift region.

192. The MIS-type semiconductor device according to claim 160, further including a drain region spaced from the first drift region.

193. The MIS-type semiconductor device according to claim 161, further including a drain region spaced from the first drift region.

194. The MIS-type semiconductor device according to claim 162, further including a drain region spaced from the first drift region.

195. The MIS-type semiconductor device according to claim 163, further including a drain region spaced from the first drift region.

196. The MIS-type semiconductor device according to claim 164, further including a drain region spaced from the first drift region.

197. The MIS-type semiconductor device according to claim 165, further including a drain region spaced from the first drift region.

198. The MIS-type semiconductor device according to claim 166, further including a drain region spaced from the first drift region.

199. The MIS-type semiconductor device according to claim 167, further including a drain region spaced from the first drift region.

200. The MIS-type semiconductor device according to claim 168, further including a drain region spaced from the first drift region.